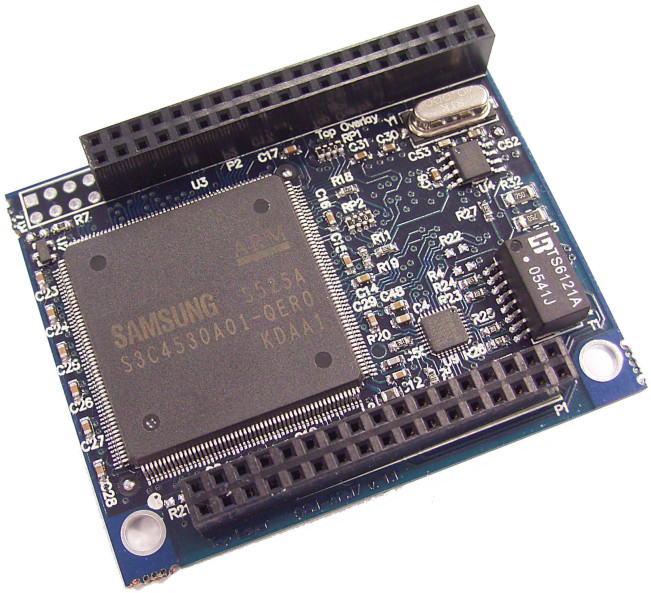


Features:

- *ARM7TDMI CPU*
- *4, 8, 16 or 32 Mbytes SDRAM*
- *2x TTL UARTs*
- *1x I2C interface*
- *1x 10 Base-T/100 Base-TX Ethernet interface*
- *1x HDLC synchronous serial interface*
- *Optional MMC/SD card socket*
- *8-bit expansion bus*
- *Small size – 64x51mm*

µClinux

-------- *Ready!*

Description:

OEM-ARM7 is a cost-effective, high-performance, small-sized single board computer (SBC). Running uCLinux, the module is suitable for large variety of applications. The set of the peripherals allows easy and seamless interface to the target system.

The module is built around the Samsung's S3C4530A network controller. The IC is based on Advanced RISC Machines, Ltd. 16/32bit RISC ARM7TDMI core, and contains peripherals suited equally well for very specific and general-purpose aplications. This includes:

- 8-Kbyte unified cache, that can be used also as general-purpose SRAM;
- I^2C interface;
- 10/100 Mbps Ethernet MAC;
- HDLC controller;
- General purpose and specialized DMA channels
- UARTs;
- Timers;
- Programmable I/O ports
- Interrupt controller;
- SDRAM controller that supports SDRAM burst mode;
- FLASH memory contoller;
- Bus controller;
- PLL.

The CPU operates at programmable frequency of up to 50 MHz, delivering performance up to 45 MIPS.

Onboard resources:

- 4, 8, 16* or 32 megabytes of RAM memory, capable of operating at zero waitstate, mapped on 16 or 32bit of the CPU bus;
- 2, 4* or 8 megabytes of NOR FLASH memory
- 10 Base-T/100 Base-TX ethernet PHY with transformer;
- connectors for stuffing the board onto the target system;
- On-board LDO regulator for larger range of operating voltage.

* This option is included in the basic configuration of the board.

On-board options:

- on U10 possition may be stuffed 24LCXXX series of I2C EEPROM;
- on P11 possition may be stuffed SD/MMC card socket type YKCO-881-1220103 by YIKUO Techology Co, Ltd.

Supplied firmware:

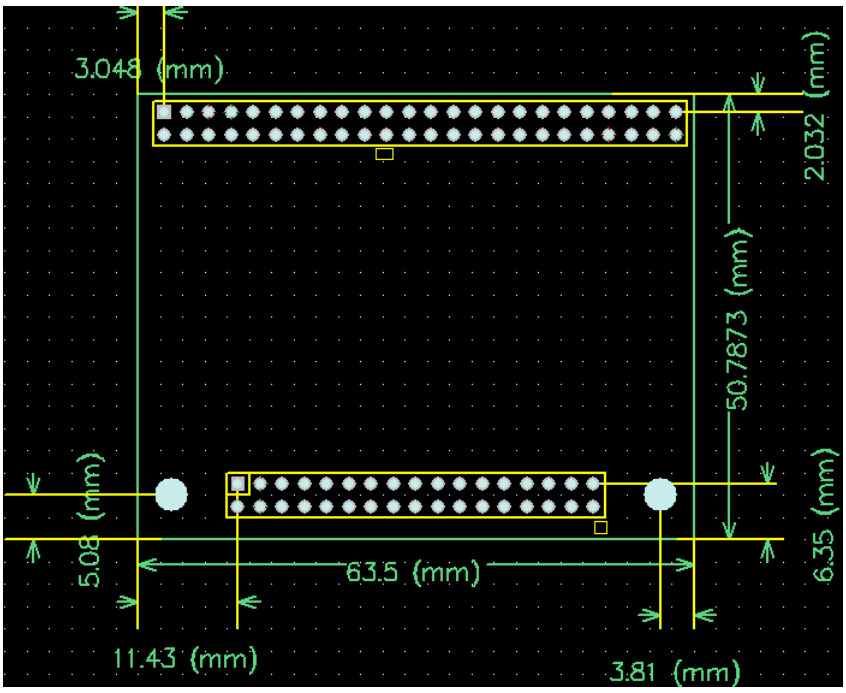
1) BIOS setup for most of the onboard functions:
   - CPU core functions;
   - FLASH memory options;
   - SDRAM memory options;
   - External Bus interface;
   - Ethernet MAC setup: TFTP server IP address and MAC address;
   - Password and boot options.

2) uClinux port with linux kernel 2.4.22-uc0:
   - jffs2 read/write flash file system;
   - basic linux command set;
   - ftp, telnet, samba services;
   - 1 megabyte free user space into the flash file system.

3) CD-ROM with development software:
   - compiler toolchain for ARM7TDMI CPU core;
   - uCLinux distribution sources for the configuration supplied on the module;
   - BIOS sources;
   - This documentation
   - Instruction on how to build and upload a new image for the kernel and filesystem;
   - Instruction on how to build and upload new BIOS.

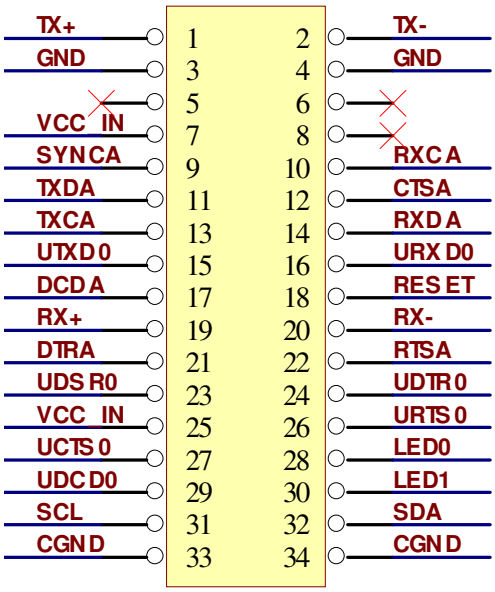
Board mechanical information:

On the following pictures are presented the physical dimensions of the board and the possition of the connectors and mounting holes:



Board electrical information:

On the following pictures is presented the electrical interface of the module:
- Connector P1 (2X17 pins), female:

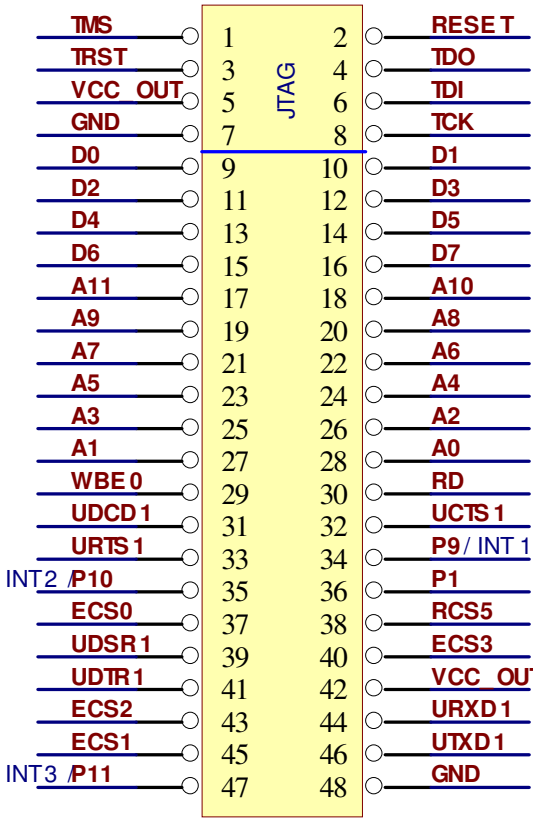


Description of the signals:

1) Ethernet line, Tx pair, positive line;
2) Ethernet line, Tx pair, negative line;
3) Digital ground;
4) Digital ground;
5) Pin not used; may be connected to some other signal or left floating;
6) Pin not used; may be connected to some other signal or left floating;
7) Input power supply positive pole;
8) Pin not used; may be connected to some other signal or left floating;
9) HDLC interface SYNC input signal;
10) HDLC interface Receive Clock input signal;
11) HDLC interface Transmit Data output signal;
12) HDLC interface Clear-To-Send output signal;
13) HDLC interface Transmit Clock output signal;
14) HDLC interface Receive Data input signal;
15) UART0 interface Transmit Data output signal;
16) UART0 interface Receive Data input signal;
17) HDLC interface Carrier Detect input signal;
18) Board RESET – open-drain, input/output active low-level signal;
19) Ethernet line, Rx pair, positive line;
20) Ethernet line, Rx pair, negative line;
21) HDLC interface Data Terminal Ready output signal;
22) HDLC interface Ready-To-Send input signal;
23) UART0 interface Data-Set-Ready input signal;
24) UART0 interface Data Terminal Ready output signal;
25) Input power supply positive pole;
26) UART0 interface Ready-To-Send input signal;
27) UART0 interface Clear-To-Send output signal;
28) Ethernet PHY LED0 (default Link LED) open-drain output;
29) UART0 interface Carrier Detect input signal;
30) Ethernet PHY LED1 (default Activity LED) open-drain output;
31) I2C interface clock line (SCL);
32) I2C interface data line (SDA);

33) Chassis ground;
34) Chassis ground;

- Connector P2 (2X24 pins), female:



Description of the signals:

1)* JTAG interface TMS signal;
2)* Board RESET signal (the same as P1/18);
3)* JTAG interface TRST signal;
4)* JTAG interface TDO signal;
5)* Power supply output positive pole – 3.3V;
6)* JTAG interface TDI signal;
7)* Digital ground;
8)* JTAG interface TCK signal;
9) Data bus D0 signal;
10) Data bus D1 signal;
11) Data bus D2 signal;
12) Data bus D3 signal;
13) Data bus D4 signal;
14) Data bus D5 signal;
15) Data bus D6 signal;
16) Data bus D7 signal;
17) Address bus A11 signal;
18) Address bus A10 signal;
19) Address bus A9 signal;
20) Address bus A8 signal;
21) Address bus A7 signal;
22) Address bus A6 signal;
23) Address bus A5 signal;

24) Address bus A4 signal;
25) Address bus A3 signal;
26) Address bus A2 signal;
27) Address bus A1 signal;
28) Address bus A0 signal;
29) Bus Write active low signal;
30) Bus Read active low signal;
31) UART1 interface Carrier Detect input signal;
32) UART1 interface Clear-To-Send output signal;
33) UART1 interface Ready-To-Send input signal;
34) P9 / INT1 general-purpose pin;
35) P10 / INT2 general-purpose pin;
36) P1 general-purpose pin;
37) ECS0 peripheral chip select signal for bus access;
38) RCS5 memory chip select signal for bus access;
39) UART1 interface Data-Set-Ready input signal;
40) ECS3 peripheral chip select signal for bus access;
41) UART0 interface Data Terminal Ready output signal;
42) Power supply output positive pole – 3.3V;
43) ECS2 peripheral chip select signal for bus access;
44) UART1 interface Receive Data input signal;
45) ECS1 peripheral chip select signal for bus access;
46) UART1 interface Transmit Data output signal;
47) P11 / INT3 general-purpose pin;
48) Digital ground.

* Note: Normally, the JTAG interface is not necessary and is not used. The default board configuration does not provide connector for pins 1-8; connector for pins 9-48 is stuffed on the board.

Electrical data:

- Power supply voltage: 3.3V-6V;
- Power consumption at 3.3V, operating at 50MHz: typically 300mA;
- All signals except Data Bus (D0-D7) signals are 5V tolerant;
- Data Bus (D0-D7) signals may be connected to 5V systems, if resistors of 50-100 ohm are serially connected between the module and the 5V system;
- I2C bus is pulled up on-board to 3.3V power rail with 2K resistors on both SCL and SDA lines;
- RESET is pulled-up onboard to 3.3V power rail with 10K resistor; on-board is present power-on reset circuit; the pulse generated for RESET at power-up may be used by off-board peripherals.

For more information, refer to datasheets of the components used to build the board:

- CPU: S3C4530A – (http://www.samsung.com/products/semiconductor/SystemLSI/Networks/PersonalNTASSP/CommunicationProcessor/S3C4530A/S3C4530A.htm)
- Ethernet PHY: 78Q2123 – (http://www.teridian.com/products/product_detail.cfm?product_key=74)
- On-board LDO (between VCC_IN and VCC_OUT): FS8860-33CJ – (http://www.fsc.com.tw/product3.asp?pno=FS8860)
- Ethernet magnetics: TS6121A – (http://www.bothhandusa.com/products/100BaseT/TS6121A-RevB4-030402.pdf)

uClinux booting:

```
OEM-ARM7 BIOS for SAMSUNG S3C4530A v1.20-lt75 (modified bios-lt)

Press Enter for Menu, Esc for Safe Mode

Initializing system .... Done
Found M29W320DB at 0x00000000

Password: ***

Main Menu

1 - BIOS Setup
2 - Run Fdisk
3 - Load Image
4 - Update Image
5 - Reboot

Please Select 3

Loading Image From Disk ............... Gunzip Ok.
Done
Linux version 2.4.22-uc0 (root@linux) (gcc version 2.95.3 20010315 (release)(ColdFire patches
- 20010318 from http://fiddes.net/coldfire/)(uClinux XIP and shared lib patches from
http://www.snapgear.com/)) #22 Sat Nov 18 13:03:52 EET 2006
Processor: Samsung S3C4510B revision 6
Architecture: SNDS100
On node 0 totalpages: 4096
zone(0): 0 pages.
zone(1): 4096 pages.
zone(2): 0 pages.
Kernel command line: root=/dev/mtdblock3
Calibrating delay loop... 49.86 BogoMIPS
Memory: 16MB = 16MB total
Memory: 15056KB available (891K code, 175K data, 40K init)
Dentry cache hash table entries: 2048 (order: 2, 16384 bytes)
Inode cache hash table entries: 1024 (order: 1, 8192 bytes)
Mount cache hash table entries: 512 (order: 0, 4096 bytes)
Buffer cache hash table entries: 1024 (order: 0, 4096 bytes)
Page-cache hash table entries: 4096 (order: 2, 16384 bytes)
POSIX conformance testing by UNIFIX
Linux NET4.0 for Linux 2.4
Based upon Swansea University Computer Society NET3.039
Initializing RT netlink socket
Starting kswapd
JFFS2 version 2.1. (C) 2001 Red Hat, Inc., designed by Axis Communications AB.
Samsung S3C4510 Serial driver version 0.9 (2001-12-27) with no serial options enabled
ttyS00 at 0x3ffd000 (irq = 5) is a S3C4510B
ttyS01 at 0x3ffe000 (irq = 7) is a S3C4510B
RAMDISK driver initialized: 16 RAM disks of 1024K size 1024 blocksize
Samsung S3C4510 Ethernet driver version 0.1 (2002-02-20) <mac@os.nctu.edu.tw>
eth0: 00:40:95:36:35:34
OEM-ARM7 flash device: 400000 at 5000000
OEM-ARM7 flash address remaped: at 5000000
Search for id:(20 22cb) interleave(1) type(2)
Found: ST M29W320DB
OEM-ARM7 flash: Found 1 x16 devices at 0x0 in 16-bit mode
number of JEDEC chips: 1
OEM-ARM7 using static partition definition
Creating 3 MTD partitions on "OEM-ARM7 flash":
0x00000000-0x00020000 : "OEM-ARM7 bios"
0x00020000-0x000c0000 : "OEM-ARM7 kernel"
0x000c0000-0x00400000 : "OEM-ARM7 jffs2"
NET4: Linux TCP/IP 1.0 for NET4.0
IP Protocols: ICMP, UDP, TCP
IP: routing cache hash table of 512 buckets, 4Kbytes
TCP: Hash tables configured (established 1024 bind 1024)
VFS: Mounted root (jffs2 filesystem) readonly.
Freeing init memory: 40K
Shell invoked to run file: /etc/rc
Command: hostname Samsung
Command: /bin/expand /etc/ramfs.img /dev/ram0
Command: mount -t proc proc /proc
Command: mount -t ext2 /dev/ram0 /var
```

```
Command: mount -n -o remount,rw /
Command: mkdir /var/config
Command: mkdir /var/tmp
Command: mkdir /var/log
Command: mkdir /var/run
Command: mkdir /var/lock
Command: mkdir /var/empty
Command: cp /etc/utmp /var/log
Command: cat /etc/motd
Welcome to
          ____ _  _
         /  __| ||_|
    _   _| |  | | _ ____  _   _  _  _
   | | | | |  | || |  _ \| | | |\ \/ /
   | |_| | |__| || | | | | |_| |/    \
   |  ___\____|_||_|_| |_|\____|\_/\_/
   | |
   |_|

For further information check:
http://www.uclinux.org/

Command: ifconfig lo 127.0.0.1
Command: route add -net 127.0.0.0 netmask 255.255.255.0 lo
Command: ifconfig eth0 192.168.0.192 up
Command: route add -net 192.168.0.0 netmask 255.255.255.0 eth0
Execution Finished, Exiting

Sash command shell (version 1.1.1)
/>
/> cat /proc/cpuinfo
Processor       : Samsung S3C4510B rev 6 (v3l)
BogoMIPS        : 49.86
Hardware        : SNDS100
Revision        : 0000
Serial          : 0000000000000000
/>
```